519867
Rec'd PCT 30 DEC 2004

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
8 January 2004 (08.01.2004)

PCT

(10) International Publication Number
WO 2004/003574 A1

(51) International Patent Classification[7]: G01R 19/165, 31/40, 31/36, G06F 1/24, 1/28

(21) International Application Number: PCT/SG2002/000148

(22) International Filing Date: 1 July 2002 (01.07.2002)

(25) Filing Language: English

(26) Publication Language: English

(71) Applicant *(for all designated States except US)*: INFINEON TECHNOLOGIES AG [DE/DE]; St.-Martin-strasee 53, 81669 Munich (DE).

(72) Inventor; and

(75) Inventor/Applicant *(for US only)*: MA, Fan, Yung [SG/SG]; 66 Jalan Girang, Singapore 359235 (SG).

(74) Agent: WATKIN, Timothy, Lawrence, Harvey; Lloyd Wise, Tanjong Pagar P.O. Box 636, Singapore 910816 (SG).

(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZM, ZW.

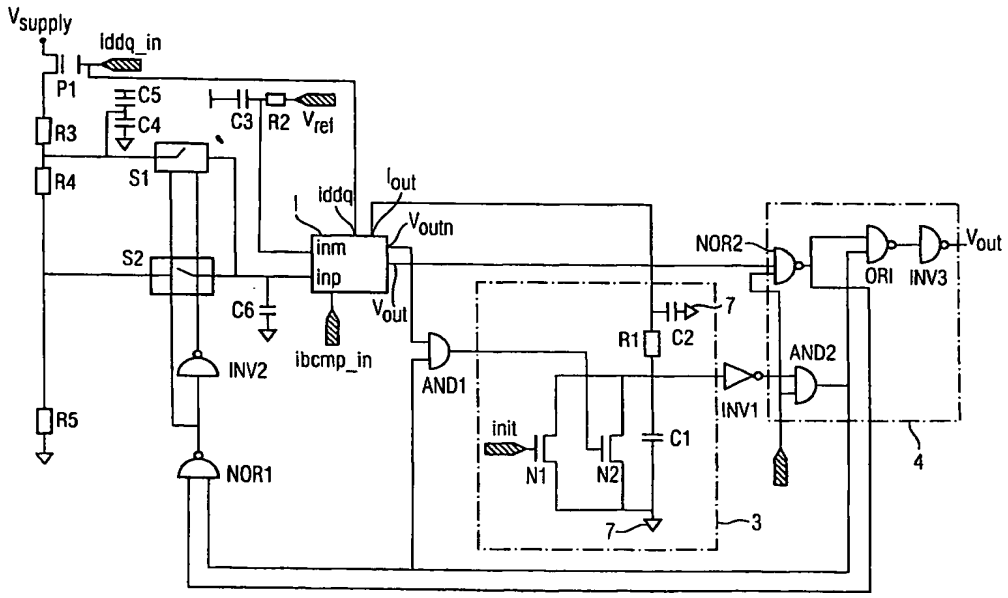
(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Declaration under Rule 4.17:
— *of inventorship (Rule 4.17(iv)) for US only*

Published:
— *with international search report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: UNDER-VOLTAGE DETECTION CIRCUIT



(57) Abstract: An under-voltage detection (UVD) circuit includes a comparator 1 for determining the amount by which a voltage supply V_{supply} falls short of a reference voltage V_{ref}, and an integrator 3 for time-integrating this shortfall. In a glitch immunce operating mode of the UVD circuit, a reset is generated using this integrated value. A reset is only generated in the case that a glitch in the supply voltage V_{supply} has a duration longer than a critical duration. The critical duration depends upon the magnitude of the glitch and the component values of the integrator 3.

WO 2004/003574 A1

Under-voltage detection Circuit

Field of the invention

The present invention relates to an under-voltage detection (UVD) circuit for a microprocessor, and to a microprocessor employing the UVD circuit.

Background of the invention

Under-voltage detection (UVD) circuits are circuits for detecting when a supply voltage falls below a detection threshold. UVDs are used extensively in micro-controller based systems, and are used especially during power-up, power-down or brown-out conditions (i.e. supply conditions such that the supply voltage is generally below the detection threshold but includes some positive glitches). When the UVD senses that the value of a supply voltage is less than the detection threshold, it triggers a reset in the microprocessor by asserting a reset signal. In certain circumstances however (such as electrostatic discharge (ESD) tests) a short duration negative transient may occur which constitutes an under-voltage but which it may be preferable for the UVD circuit to ignore, so that a reset is not triggered.

It is believed that early microprocessor designs addressed this problem using an external capacitor connected near the supply pin to remove any supply glitches. Another way to achieve the same result would be to add an RC network within the microprocessor at the input of the voltage detection comparator. However, to provide a high level of glitch immunity requires large RC values, which is area intensive and therefore not suitable for IC implementation.

Summary of the invention

The present invention seeks to provide a new and useful UVD circuit, and a microprocessor having such a circuit.

In general terms, the invention proposes that a UVD circuit integrates the difference between the supply voltage and a reference signal, and determines whether a reset should be generated using this integrated signal.

Specifically, the invention may be expressed as a UVD circuit for monitoring a supply voltage and which includes:

a comparator for generating a shortfall signal indicative of a shortfall of the supply voltage in relation to a reference voltage, and

an integrator for time-integrating the shortfall signal to form an integrated signal,

wherein the output of the integrator is used to generate a reset signal.

The integrated signal may itself constitute the reset signal which is transmitted directly to reset means for resetting the microprocessor. Alternatively, the integrated signal may be just a single input to a discriminator circuit which is arranged to generating the reset signal in dependence on (but not exclusively determined by) the integrated signal.

Preferably, the shortfall signal is a current signal having a value which increases with the shortfall of the supply voltage in relation to the reference voltage. In this case the integrator may be implemented straightforwardly as a analogue circuit including a capacitance. The comparator may optionally additionally generate a voltage signal indicative of the shortfall of the supply voltage in relation to the reference voltage, and this too may be used by the discriminator.

Brief description of the figures

An embodiment of the invention will now be described in detail for the sake of example only, with reference to the following figures in which:

Fig. 1 is a schematic diagram of the UVD circuit of the embodiment;

Fig. 2 is a circuit diagram of the comparator of Fig. 1;

Fig. 3 is a circuit diagram of the embodiment;

Fig. 4 shows the current output of the comparator for a range of differences between the two input voltages;

Fig. 5, which is composed of Figs. 5(a) and 5(b), shows the response of the embodiment to two different supply voltage profiles;

Fig. 6 shows the operation of the embodiment during slow power up and power down; and

Fig 7 shows the minimum glitch duration required to trigger the embodiment in relation to the glitch magnitude.

Detailed Description of the Embodiment

A schematic view of the embodiment is shown in Fig. 1. A comparator unit 1 receives two inputs: V_{supply}, which is the power supply voltage to be checked; and V_{ref} which is the reference voltage. It produces two outputs: V2V and V2I. V2I is a current which rises with (for example, may be proportional to) the shortfall of V_{supply} compared to V_{ref}. V2V is a voltage which rises with this shortfall (for example it may be proportional to V2I).

Of these, the output V2I is transmitted to an integrator unit 3, which integrates V2I and produces a reset signal, R.

Optionally R may be transmitted directly to reset means (which are not shown, but which may be of any conventional design) which reset the microprocessor/computer system. Alternatively, a discriminator (not shown)

may be arranged to receive V2I (and optionally other inputs, such as control signals or V2V), and to generate a modified reset signal for transmission to the reset means.

Detailed circuit diagrams of a possible comparator 1 and of its connection to the integrator 3 are given by Figs. 2 and 3 respectively.

To begin with, we give an overview of Fig. 3. The comparator 1 receives two input voltage signals inm and inp which are respectively derived from a voltage reference signal V_{ref} and the voltage supply V_{supply}. The comparator generates a current output i_{out} and two voltage outputs V_{outn} and its inverse V_{outp}. As described below, i_{out} corresponds to V2I in Fig. 1, and is a current measure of the shortfall of inp in comparison to inm.

The current signal i_{out} is transmitted to the integrator 3, which produces an output signal V_o. A discriminator circuit 4 processes result V_o to generate a voltage which is a modified reset signal R_{out} (a reset is triggered when this signal is low).

Referring now in more detail to Fig. 2, the comparator 1 is a transconductance amplifier circuit with current output i_{out} and voltage outputs v_{outn} and v_{outp}. The input differential pair is constituted by the transistors P2 and P3, which respectively receive the inputs inm and inp. This differential pair and the bias transistor P0 perform a voltage to current conversion to generate signal i_{out}.

It is well-known that, for $V_{id} < \sqrt{2I_{ss}/\beta}$ the difference of the drain currents of the transistor input devices P2, P3 can be described by the equation:

$$I_{dp3} - I_{dp2} = V_{id}\sqrt{\beta I_{ss}(1 - \beta V_{id}^{\ 2}/4I_{ss})}$$

where V_{id}=inp-inm, I_{ss} is the differential pair bias current (i.e. the current through transistor P0) and is a function of the device mobility, aspect ratio and gate oxide capacitance.

This equation is mirrored to the output, i.e. the comparator output i_{out} is governed by the same equation scaled by a gain factor determined by the gain factors of the transistors N4, N5, N3, P4, and P6. Therefore, according to the equation, i_{out} varies approximately linearly with V_{id} near $V_{id}=0$, and then saturates at higher positive and negative values of I_{ss}. Therefore, prior to output current saturation this circuit approximates a linear voltage-to-current converter. The current-voltage profile is as shown in Fig. 4. The output is also used to generate a corresponding voltage output V_{out} and its inverse V_{outn}.

Iddq is a power down signal which goes high to indicate that there will be a power down. Pbias is generated by a bias circuit (which is not shown in Fig. 3).

Turning back to Fig. 3, the integrator 3 is composed of a resistor R1 and two capacitors C1 and C2. It can be derived that for a unit step input applied at the input (from the i_{out} of the comparator), the output voltage V_o at the input of the inverter INV1 follows the equation:

$$V_o = k\left(t - \tau\left(1 - \exp\left(-t/\tau\right)\right)\right)u(t)$$

where

$$k = i_{out}/(C1 + C2)$$

and

$$\tau = R1 * C1 * C2/(C1 + C2)$$

Also, *exp* is the natural logarithm exponential function, and *u(t)* is the unit step function. Basically, V_o has an approximately linear relationship with time. The integrator 3 thus performs an integration function, and the integrated voltage causes INV1 to change its state when its trip point is reached, thus generating a reset signal.

The discriminator 4 of Fig. 3 is controlled by an input signal *en* and permits both glitch immune (en="1") and glitch sensitive (en="0"). In the glitch immune case, the AND gate AND2 transmits the output of the inverter INV1,

this is transmitted through the OR gate OR1, and inverted by the inverter INV3. Thus, there is a low output (a modified reset signal which triggers a reset in the reset means) whenever the output of the integrator 3 is higher than the trip voltage V_c of the inverter INV1 and vice versa. In the glitch sensitive case, *en* is low and the output of the UVD circuit is determined instead by V_{out} (since the output of the AND gate AND0 is always zero). Specifically, R_{out} is high (low) when V_{out} is high (low).

The configuration of the other components of Fig. 3 will be understood by a skilled reader. Transistor P1, resistors R3, R4 and R5, provide a scaled version of the supply voltage Vsupply. Capacitors C4, C5 and C6, provide some limited fast glitch immunity using standard RC effects. To provide more glitch immunity using such techniques would however require large values of RC which is area intensive and not practical for IC implementation.

Resistor R2 and capacitor C3 provide a low-pass filter for the comparator reference signal to remove any effects of jitter in this signal.

Switches S1 and S2, together with gates NOR1 and INV2 are arranged to provide hysteresis in the detection. According to which of the switches S1 and S2 is turned on, the input inp is scaled. This means that the effective supply voltage seen by the comparator 1 can be higher or lower according to whether the reset has already been triggered.

Gate AND1 and transistor N2 are used to discharge C1 by connecting it to ground 7 once the input to INV1 decreases past the INV1 trip point. This is to prepare the circuit for the next positive event, e.g. power-up.

Transistor N1 and the input init are used to initialise the voltage across C1 to ground upon power-up. Normally, init is low, so that the transitor N1 is

inactive, but upon an initialisation of the UVD circuit init is set to high, to ground C1.

Fig. 5(a) shows schematically the time variation of the circuit in two cases, for both of which the UVD circuit is in the glitch immune state. In the case of Fig. 5(a) the supply voltage V_{supply} falls below V_{ref} for a short time indicated by the shaded area 5. V_o is high before this time, but during period 5 falls roughly in proportion to the time the glitch has lasted. However, Vsupply rises above Vref before the inverter INV1 is tripped, so the output R_{out} remains at logic one, and there is no reset.

Conversely, in the case shown in Fig. 5(b), however, V_{supply} is below V_{ref} for sufficiently long that V_o falls below the trip voltage V_c of the inverter INV1, and R_{out} falls to zero, i.e. there is a reset.

Fig. 6 shows the variation of R_{out} with time during a slow power-up and power-down.

Fig. 7 shows, for typical component values in the circuits of Figs. 2 and 3, the minimum duration of a glitch which will cause a reset for glitches of differing magnitudes (i.e. differing values of the shortfall of V_{supply} in relation to V_{ref}) in the glitch immune state of the UVD circuit. The magnitude of the glitches is given on the x-axis, while the time that such a glitch must last in order to cause a reset is shown on the y-axis. As can be seen from Fig. 7 a glitch of more than about 650mV will cause a reset irrespective of its duration. For a wide range of glitch magnitudes (say 250mV to 600mV) a reset will only be caused if the duration of the glitch is more than about 7 μs.

Although only a single embodiment of the invention has been described in detail, various modifications are possible within the scope of the invention as will be clear to a skilled reader.

5

Claims

1. A UVD circuit for monitoring a supply voltage and which includes:

a comparator for generating a shortfall signal indicative of a shortfall of the supply voltage in relation to a reference voltage, and

an integrator for time-integrating the shortfall signal to form an integrated signal,

wherein the output of the integrator is used to generate a reset signal.

2. A UVD circuit according to claim 1 further including a discriminator circuit for receiving the integrated signal and at least one further output of the comparator, and generating a reset signal using the integrated signal and the at least one further output.

3. A UVD circuit according to claim 2 in which the discriminator circuit is arranged to receive a control signal, the discriminator circuit further comprising a switch controlled by the control signal for determining whether the reset signal is generated based on the integrated signal or the at least one further output signal.

4. A microprocessor incorporating a UVD circuit according to any preceding claim, and reset means arranged to receive the reset signal output by the UVD circuit and according to its value to initiate a reset of the microprocessor.

5. A method of monitoring a supply voltage including:

generating a shortfall signal indicative of a shortfall of the supply voltage in relation to a reference voltage;

time-integrating the shortfall signal to form an integrated signal; and

generating a reset signal using the shortfall signal.

FIG 1

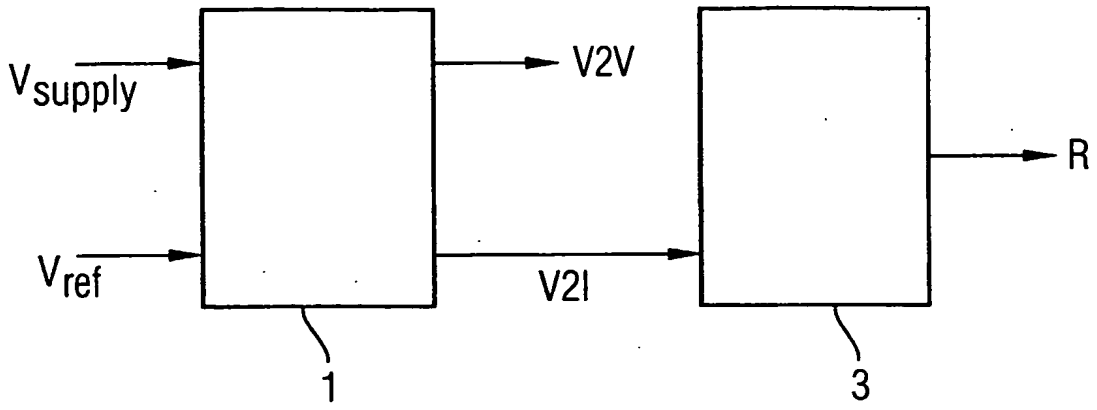
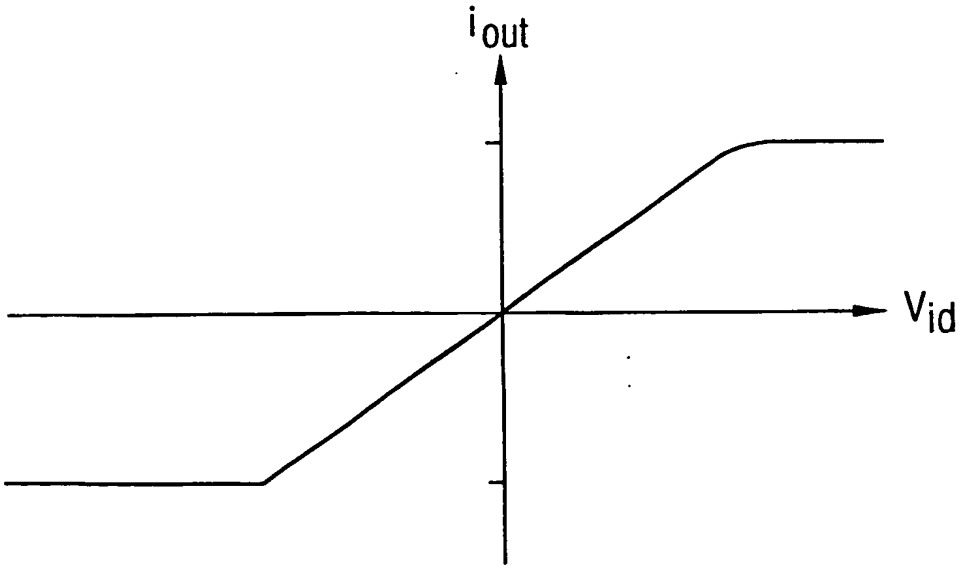


FIG 4



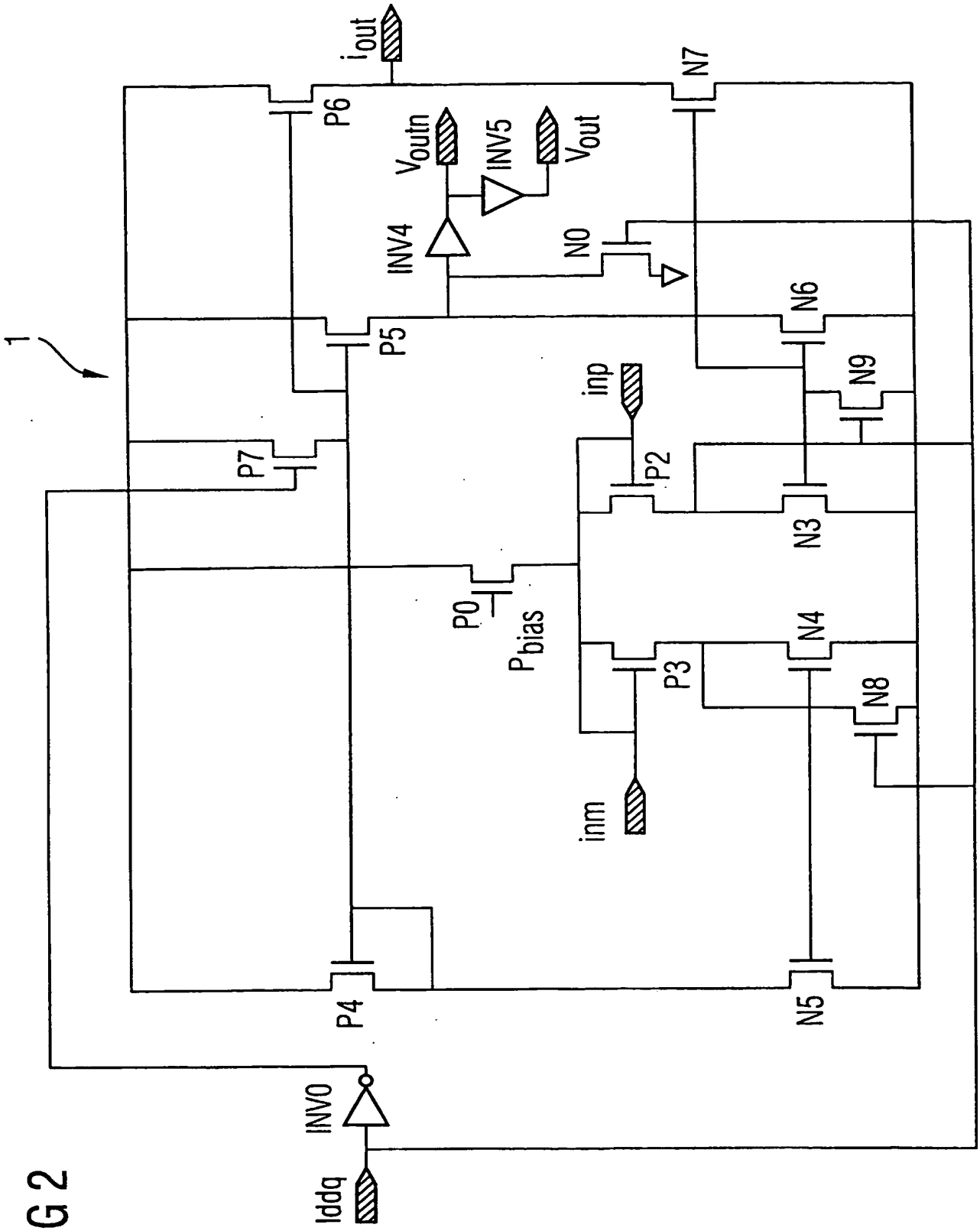

1
i_{out}
P6
N7
V_{outn}
INV5
V_{out}
INV4
N0
N6
P5
N9
inp
P7
P2
N3
P0
P_{bias}
N4
P3
N8
inm
P4
N5
INV0
Iddq

FIG 2

FIG 3

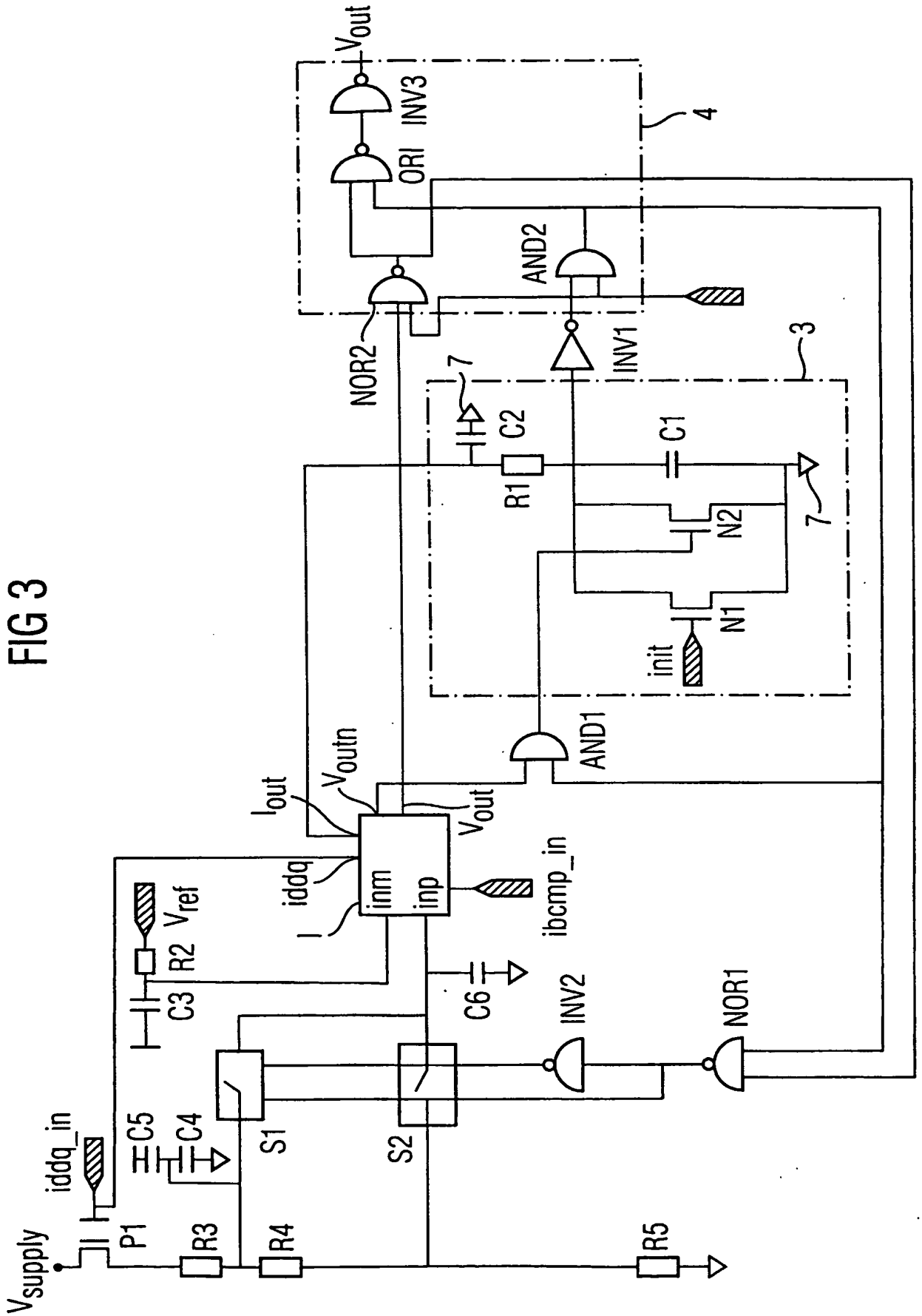

Vout
INV3
ORI
4
AND2
NOR2
INV1
3
7
C2
C1
R1
N2
N1
init
AND1
Iout
Voutn
idda
inm
inp
ibcmp_in
Vref
R2
C3
C6
INV2
NOR1
C5
C4
S1
S2
idda_in
P1
R3
R4
R5
Vsupply

FIG 5A

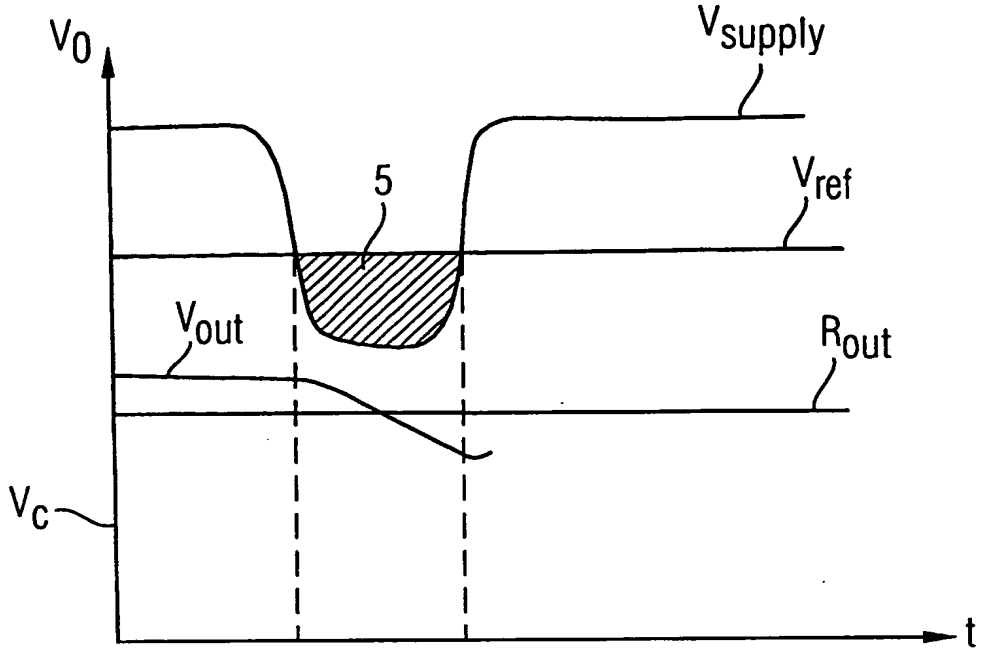


FIG 5B

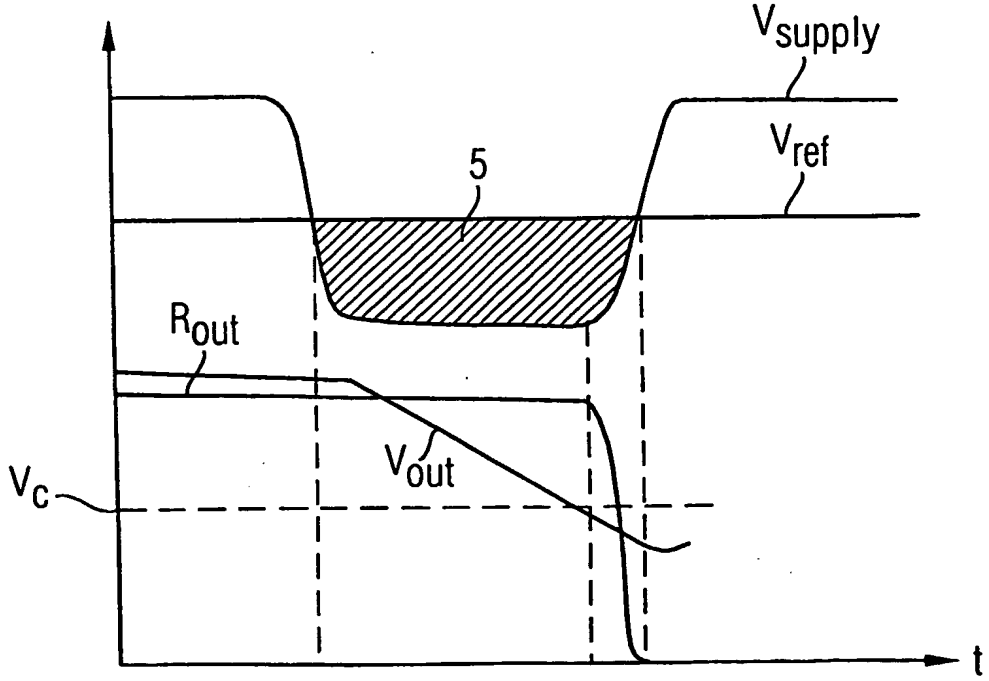


FIG 5

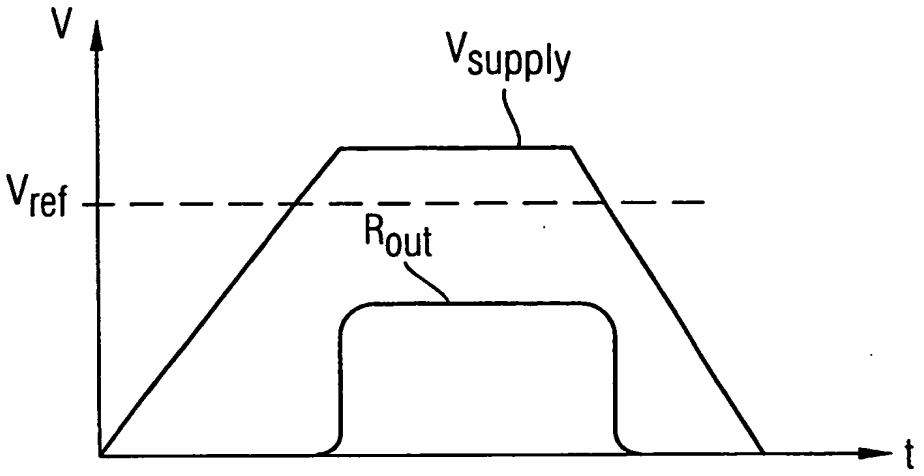
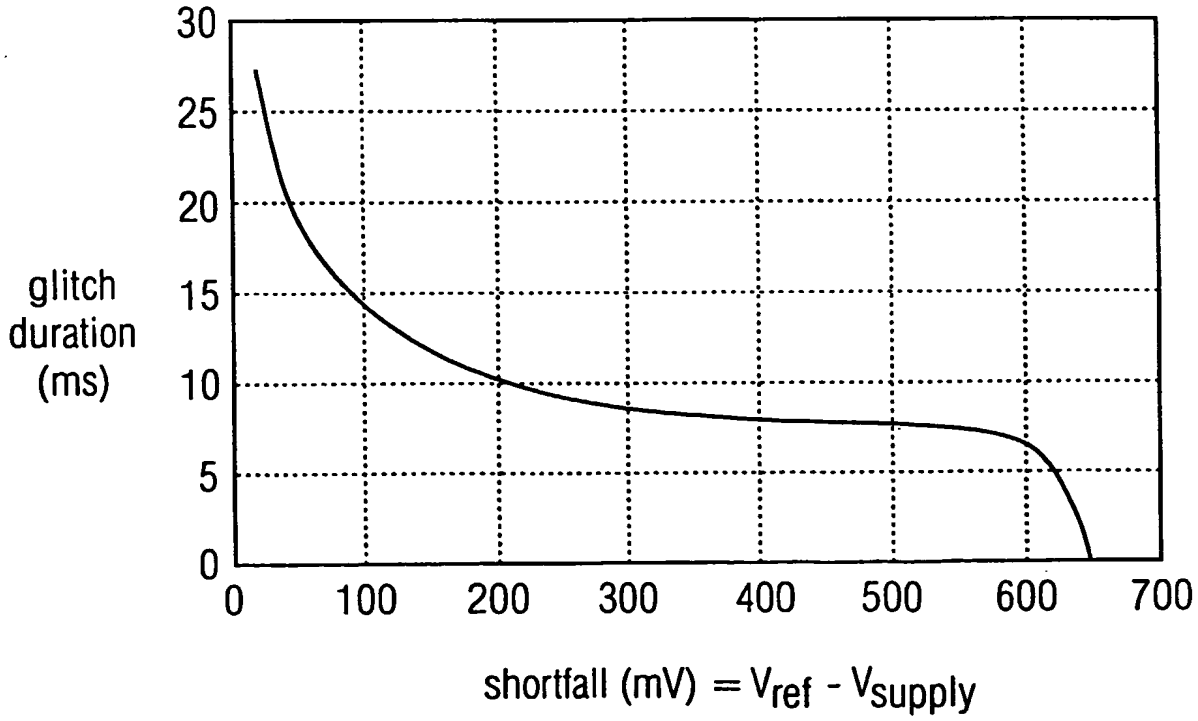

V
V_{supply}
V_{ref}
R_{out}
t

FIG 6


30
25
20
15
10
5
0
glitch duration (ms)
0
100
200
300
400
500
600
700
shortfall (mV) = V_{ref} - V_{supply}

INTERNATIONAL SEARCH REPORT

International Application No
PCT/SG 02/00148

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G01R19/165 G01R31/40 G01R31/36 G06F1/24 G06F1/28

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G01R G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, PAJ, INSPEC, IBM-TDB

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 1 037 065 A (ST MICROELECTRONICS SRL) 20 September 2000 (2000-09-20) column 3, line 36 -column 4, line 31; figure 1	1,5
A	---	2-4
A	US 4 429 236 A (NITSCHKE WERNER) 31 January 1984 (1984-01-31) abstract column 1, line 10 - line 16 column 2, line 4 - line 51; figure 1	1-5

A	US 5 539 910 A (BRUECKMANN DIETER ET AL) 23 July 1996 (1996-07-23) abstract column 1, line 9 - line 38 column 3, line 9 -column 5, line 56; figure 1	1-5

	-/--	

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
28 April 2003	09/05/2003

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Bergado Colina, J

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

International Application No
PCT/SG 02/00148

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
A	US 4 224 539 A (MUSA FUAD H ET AL) 23 September 1980 (1980-09-23) column 2, line 4 - line 31; figure 1 column 2, line 32 -column 3, line 31; figure 2 ---	1-5
A	US 5 099 209 A (SEKI YOICHI ET AL) 24 March 1992 (1992-03-24) column 2, line 27 -column 4, line 67; figure 1 ---	1-5
A	US 3 789 236 A (LACROIX P) 29 January 1974 (1974-01-29) abstract column 1, line 4 - line 9 column 1, line 66 -column 3, line 37; figure 1 ---	1-5
A	WO 02 29701 A (SIEMENS AG ;TYROLLER TOBIAS (DE)) 11 April 2002 (2002-04-11) abstract page 3, line 25 -page 5, line 25; figures 1,2 -----	1-5

INTERNATIONAL SEARCH REPORT

International Application No
PCT/SG 02/00148

Patent document cited in search report		Publication date	Patent family member(s)		Publication date
EP 1037065	A	20-09-2000	EP	1037065 A1	20-09-2000
			JP	2000241515 A	08-09-2000
			US	6339315 B1	15-01-2002
US 4429236	A	31-01-1984	DE	3035896 A1	06-05-1982
			FR	2490829 A1	26-03-1982
US 5539910	A	23-07-1996	DE	4314533 C1	19-05-1994
			EP	0623868 A1	09-11-1994
US 4224539	A	23-09-1980	DE	2935858 A1	13-03-1980
			FR	2435723 A1	04-04-1980
			GB	2030398 A ,B	02-04-1980
			JP	55149879 A	21-11-1980
			MY	71786 A	31-12-1986
US 5099209	A	24-03-1992	JP	2667993 B2	27-10-1997
			JP	3131771 A	05-06-1991
			DE	4032842 A1	25-04-1991
			GB	2237115 A ,B	24-04-1991
US 3789236	A	29-01-1974	FR	2148946 A5	23-03-1973
			AT	317363 B	26-08-1974
			AU	474265 B2	15-07-1976
			AU	4521972 A	07-02-1974
			BE	787328 A1	08-02-1973
			DE	2239268 A1	01-03-1973
			ES	405657 A1	01-07-1975
			GB	1397594 A	11-06-1975
			IT	964864 B	31-01-1974
			LU	65869 A1	08-02-1973
			NL	7210641 A	13-02-1973
			PL	78188 B1	30-04-1975
WO 0229701	A	11-04-2002	WO	0229701 A1	11-04-2002